LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (previously presented) A power conversion circuit, comprising:

an unregulated isolated board mounted power module operable to convert a nominal input voltage into an intermediate bus voltage, the isolated board mounted power module having at least one pair of MOSFETS connected in series in a bridge configuration across the nominal input voltage, the power module being operated in an open-loop,

a primary open-loop inversion circuit having

a controller IC for driving the at least one pair of MOSFETS, the controller IC being operable to alternatively control the pair of MOSFETS with a 50% duty cycle, and

a timing resistor and a timing capacitor, wherein a dead-time and a switching frequency of the controller IC being adjustable in accordance with values of the timing resistor and the timing capacitor; and

a plurality of tightly regulated point-of-load converters operable to convert the intermediate bus voltage into respective point-of-load voltages to power a respective number of loads.

2. (currently amended) The power conversion circuit of claim 1, wherein the board mounted power module includes

[[a]]the primary open-loop inversion circuit,

a primary bias circuit,

a secondary synchronous rectification and filtering circuit, and

a secondary bias circuit magnetically coupled to one another, the synchronous rectification and filtering circuit producing the intermediate bus voltage.

3. (currently amended) The power conversion circuit of claim 2, wherein the ~~primary open-loop inversion circuit includes~~ controller IC is a half-bridge controller IC for driving the pair of MOSFETS connected in a half-bridge configuration~~, the controller IC being operable to~~

~~alternatively control the pair of MOSFETS with a 50% duty cycle~~.

4. (cancelled)

5. (currently amended) The power conversion circuit of claim [[4]]3, wherein the switching frequency is determined by the formula $f_s = \frac{1}{2R_1C_2}$, where fs is the switching frequency, R1 is the value of the timing resistor, and C2 is the value of the timing capacitor.

6. (original) The power conversion circuit of claim 3, wherein the pair of MOSFETS include DirectFETs.

7. (original) The power conversion circuit of claim 3, wherein the half-bridge controller IC may be run in at least two modes, one of the modes being a self-oscillating mode, another one of the modes being a synchronized mode.

8. (currently amended) The power conversion circuit of claim 2, wherein the ~~primary open-loop inversion circuit includes~~ controller IC is a full-bridge controller IC and two pairs of MOSFETS connected in a full bridge configuration~~, the controller IC being operable to alternatively control the two pair of MOSFETS with a 50% duty cycle~~.

9. (original) The power conversion circuit of claim 8, wherein the primary open-loop inversion circuit includes a timing resistor and a timing capacitor, a dead-time and switching frequency of the full-bridge controller IC being adjustable in accordance with values of the timing resistor and the timing capacitor.

10. (original) The power conversion circuit of claim 9, wherein the switching frequency is determined by the formula $f_s = \frac{1}{2R_1C_2}$, where fs is the switching frequency, R1 is the value of the timing resistor, and C2 is the value of the timing capacitor.

11. (original) The power conversion circuit of claim 8, wherein the two pairs of MOSFETS include DirectFETs.

12. (previously presented) The power conversion circuit of claim 8, wherein the full-bridge controller IC may be run in at least two modes, one of the modes being a self-oscillating mode, another one of the modes being a synchronized mode.

13. (currently amended) A half-bridge controller IC for use with a power conversion circuit including an isolated unregulated board mounted power module operable to convert a nominal input voltage into an intermediate bus voltage[[;]], the board mounted power module being operated in an open-loop[[;]], and a plurality of tightly regulated point-of-load converters operable to convert the intermediate bus voltage into respective point-of-load voltages to power a respective number of loads, the half-bridge controller IC comprising:

a biasing circuit to produce a bias voltage to operate the half-bridge controller IC;

under-voltage lock-out circuit operable to monitor a voltage on a power supply pin of the half-bridge controller IC;

an oscillator circuit to provide a timing signal having a 50% duty cycle;

a soft-start circuit to ensure that the duty cycle of the timing signal increases gradually from zero to the 50% duty cycle to ease in-rush current during start-up; and

high-side and low-side drivers to provide MOSFET driving signals to control a pair of MOSFETS connected to one another in series in a half-bridge configuration across the nominal input voltage, the half-bridge controller IC alternatively controlling the MOSFETS with a 50% duty cycle, wherein the unregulated isolated board mounted power module includes

a primary open-loop inversion circuit,

a primary bias circuit,

a secondary rectification and filtering circuit,

a secondary bias circuit, the primary open-loop inversion circuit being magnetically coupled to the secondary rectification and filtering circuit, the primary bias circuit being magnetically coupled to the secondary bias circuit, the secondary rectification and filtering circuit producing

the intermediate bus voltage.

14. (original) The half-bridge controller IC of claim 13, wherein the MOSFETS include a pair of DirectFETs.

15. (currently amended) A power conversion circuit, comprising:

an unregulated isolated board mounted power module operable to convert a nominal input voltage into an intermediate bus voltage, the isolated board mounted power module being operated in an open-loop, the unregulated isolated board mounted power module including

a primary open-loop inversion circuit,

a primary bias circuit,

a secondary rectification and filtering circuit,

a secondary bias circuit, the primary open-loop inversion circuit being magnetically coupled to the secondary rectification and filtering circuit, the primary bias circuit being magnetically coupled to the secondary bias circuit, the secondary rectification and filtering circuit producing the intermediate bus voltage, and

a half-bridge controller IC, the half-bridge controller IC including

a biasing circuit to produce a bias voltage to operate the half-bridge controller IC,

under-voltage lock-out circuit operable to monitor a voltage on a power supply pin of the half-bridge controller IC,

an oscillator circuit to provide a timing signal having a 50% duty cycle,

a soft-start circuit to ensure that the duty cycle of the timing signal increases gradually from zero to the 50% duty cycle to ease in-rush current during start-up, and

high-side and low-side drivers to provide MOSFET driving signals to control a pair of MOSFETS connected to one another in series in a half-bridge configuration across the nominal input voltage, the half-bridge controller IC alternatively controlling the MOSFETS with a 50% duty cycle; and

a plurality of tightly regulated point-of-load converters operable to convert the intermediate bus voltage into respective point-of-load voltages to power a respective number of loads.

16. (cancelled)

17. (currently amended) The power conversion circuit of claim [[16]]15, wherein the primary open-loop inversion circuit includes a timing resistor and a timing capacitor, a dead-time and switching frequency of the controller IC being adjustable in accordance with values of the timing resistor and the timing capacitor.

18. (original) The power conversion circuit of claim 17, wherein the switching frequency is determined by the formula $f_s = \frac{1}{2R_1C_2}$, where fs is the switching frequency, R1 is the value of the timing resistor, and C2 is the value of the timing capacitor.

19. (currently amended) The power conversion circuit of claim [[16]]15, wherein the pair of MOSFETS include DirectFETs.

20. (currently amended) The power conversion circuit of claim [[16]]15, wherein the half-bridge controller IC may be run in at least two modes, one of the modes being a self-oscillating mode, another one of the modes being a synchronized mode.

21. (currently amended) The power conversion circuit of claim [[4]]3, wherein the switching frequency fs is inversely proportional to R1, the value of the timing resistor, and C2, the value of the timing capacitor.

22. (previously presented) The power conversion circuit of claim 9, wherein the switching frequency fs is inversely proportional to R1, the value of the timing resistor, and C2, the value of the timing capacitor.

23. (previously presented) The power conversion circuit of claim 17, wherein the switching frequency fs is inversely proportional to R1, the value of the timing resistor, and C2,

the value of the timing capacitor.

24. (previously presented) The power conversion circuit of claim 13, wherein the board mounted power module includes a primary open-loop inversion circuit, a primary bias circuit, a secondary rectification and filtering circuit, and a secondary bias circuit, the primary open-loop inversion circuit being magnetically coupled to the secondary rectification and filtering circuit, the primary bias circuit being magnetically coupled to the secondary bias circuit, the secondary rectification and filtering circuit producing the intermediate bus voltage.

25. (previously presented) The power conversion circuit of claim 24, wherein the primary open-loop inversion circuit includes a timing resistor and a timing capacitor, a dead-time and switching frequency of the controller IC being adjustable in accordance with values of the timing resistor and the timing capacitor.

26. (previously presented) The power conversion circuit of claim 25, wherein the switching frequency is determined by the formula $f_s = \frac{1}{2R_1C_2}$, where fs is the switching frequency, R1 is the value of the timing resistor, and C2 is the value of the timing capacitor.

27. (previously presented) The power conversion circuit of claim 25, wherein the switching frequency fs is inversely proportional to R1, the value of the timing resistor, and C2, the value of the timing capacitor.